CLAIM AMENDMENTS

1. (currently amended) An on-chip differential multiple layer inductor comprises:

a first node on a first layer of a plurality of metal layers of an integrated circuit;

a second node on the first layer; and

a multi-layer winding on at least some of the plurality of metal layers, wherein the multi-layer winding is coupled to the first and second nodes, wherein the multi-layer winding is symmetrical with respect to the first and second nodes, and wherein metalization of the winding on each of the at least some of the plurality of metal layers is in an approximate range of twenty to eighty percent.
~~first partial winding on multiple first layers, wherein the first partial winding is operably coupled to receive a first leg of a differential input;~~

~~second partial winding on the multiple first layers, wherein the second partial winding is operably coupled to receive a second leg of the differential input;~~

~~third partial winding on multiple second layers, wherein the third partial winding is operably coupled to a center tap;~~

~~fourth partial winding on the multiple second layers, wherein the fourth partial winding is operably coupled to the center tap; and~~

~~interconnecting structure operably coupled to the first, second, third, and fourth partial windings such that the first and third partial windings form a winding that is symmetrical to a winding formed by the second and fourth partial windings.~~

2. (currently amended) The on-chip differential multiple layer inductor of claim 1, wherein the multi-layer winding ~~further~~ comprises:

first partial winding on at least one of the at least some of the plurality of metal layers; and

second partial winding on at least another one of the at least some of the plurality of metal layers, wherein positioning of the second partial winding with respect to positioning of the first partial winding establishes a parasitic capacitance that, in combination with inductance of the on-chip differential multiple layer inductor, provides a resonant frequency of approximately twice an operating frequency of the on-chip differential multiple layer inductor

~~the third partial winding being positioned with respect to the first partial winding and the fourth partial winding being positioned with respect to the second partial winding to establish a tuned capacitance such that a quality factor of the on-chip differential multiple layer inductor is optimized~~.

3. (currently amended) The on-chip differential multiple layer inductor of claim 2, wherein the multi-layer winding ~~1, wherein the interconnecting structure further~~ comprises:

the at least one of the at least some of the plurality of metal layers is an adjacent metal layer to the at least another one of the at least some of the plurality of metal layers, wherein the positioning of the first partial winding is offset from the positioning of the second partial winding.

~~a first set of interconnections for coupling the first partial winding to the third partial winding; and~~

~~a second set of interconnections for coupling the second partial winding to the fourth partial winding, wherein the first set of interconnections is symmetrical to the second set of interconnections.~~

4. (currently amended) The on-chip differential multiple layer inductor of claim ~~1 further comprises at least one of~~ 2, wherein the multi-layer winding comprises:

an unused metal layer of the plurality of the metal layers, wherein the unused metal layer is between the at least one of the at least some of the plurality of metal layers and the at least another one of the at least some of the plurality of metal layers, wherein the positioning of the first partial winding is aligned with the positioning of the second partial winding.

~~the first partial winding including a notched corner to provide clearance for a bridge of the interconnecting structure; and~~

~~the second partial winding including a second notched corner to provide clearance for a second bridge of the interconnecting structure.~~

5. (currently amended) The on-chip differential multiple layer inductor of claim 1 further comprises:

the at least some of the plurality of metal layers including thicker metalization layers.

~~the third partial winding having similar metalization as the first partial winding; and~~

~~the fourth partial winding having similar metalization as the second partial winding, such that yield of integrated circuits incorporating the on-chip differential multiple layer inductor increases.~~

6. (new) The on-chip differential multiple layer inductor of claim 1 further comprises:

a center tap coupled to the multi-layer winding such that the multi-layer winding is symmetrical about the center tap with respect to the first and second nodes.